UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,209	11/16/2001	Eiki Hashimoto	NEKU 19.181	5984

26304 7590 10/08/2004

KATTEN MUCHIN ZAVIS ROSENMAN
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER	
THOMPSON, ANNETTE M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,209	HASHIMOTO, EIKI	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,4,5,7,9,10,16,18 and 19* is/are allowed.

6)☒ Claim(s) *1,3,6,8,11-13,15,17 and 20* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2001 and 17 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

~~Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).~~

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's amendment to 10/015,209 has been examined. Claims 1-20 are amended. Claims 1-20 are pending.

1. Applicant's amendment is persuasive in part. However, upon reconsideration, this second non-final action based upon the existence of new prior art is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of claims 1, 3, 6, 8, 11-13, 15, 17, 20

3. Claims 1, 3, 6, 8, 11-13, 15, 17, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto et al., U.S. Patent 5,933,350. Fujimoto discloses a semiconductor device development integrating system that stores and manages electronic data created in a semiconductor device design process. Fujimoto, however, does not use the terminology inspection item or logical design. Based on the function of these units as disclosed by Applicant, a correlation may be made with the Fujimoto elements that one would have been obvious to one of ordinary skill at the time of Applicant's invention albeit the use of different terminology.

4. Pursuant to claim 1, [A] semiconductor circuit designing apparatus, comprising a circuit design unit which executes a logical design of a semiconductor integrated circuit (Fig. 1, #102; Fig. 2b, #10); and an inspection item database section (col. 6, ll. 4-7,

database 3) in which a circuit feature of said semiconductor integrated corresponds to at least one inspection item of an inspection to be executed before layout design of said semiconductor integrated circuit is executed (Fig. 1, #104), wherein said circuit design unit generates circuit feature information indicating said circuit feature of said semiconductor integrated circuit for which said logical design should be executed (col. 6, ll. 56-65; see also col. 13, ll. 23-48), wherein said circuit design unit obtains a certain inspection of said at least one inspection item corresponding to said circuit feature information from said inspection item database section (col. 7, ll. 10-17; col. 13, ll. 23-48), and wherein said circuit design unit executes said logical design of said semiconductor integrated circuit in reference to said certain inspection item (col. 7, line 66 to col. 8, line 19).

5. Pursuant to claim 3, which further comprises a layout design unit executing said layout design (Fig. 2b; manufacture section), wherein said circuit design unit executes said inspection of said target semiconductor integrated circuit for which said layout design is executed (col. 13, ll. 23-47), with regard to said certain inspection item, and wherein said circuit design unit provides a result of said inspection of said semiconductor integrated circuit to said layout design unit (col. 7, ll. 56-65).

6. Pursuant to claims 6, wherein said inspection item database section is connected to said circuit design unit (col. 6, ll. 56-65; Figs. 2a, 2b).

7. Pursuant to claims 8 and 11, wherein said inspection item database section is connected to said layout design unit (Figs. 2a, 2b, Fig. 8, Fig. 15)

8. Pursuant to claim 12, further comprising a data center (Fig. 2a, #1-3) distinct from said circuit design unit and said layout design unit (Fig. 2b, #100), wherein said inspection item database section is connected to said data center.

9. Pursuant to claim 13, which recites [a] semiconductor circuit designing method comprising (a) providing an inspection item database in which a circuit feature of a semiconductor integrated circuit for which a logical design should be executed corresponds to an inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed (col. 6, ll. 4-7); notifying a circuit designer executing said logical design of said semiconductor integrated circuit of said inspection item, retrieved from said inspection item database section, said inspection item corresponding to said circuit feature of said semiconductor integrated circuit (col. 7, ll. 56-65); and executing said logical design of said semiconductor integrated circuit by said circuit designer with reference to said notified inspection item (col. 7, ll. 56-65).

10. Pursuant to claim 15, which recites (a) providing a circuit design unit executing a logical design of a semiconductor integrated circuit (Fig. 1, #102; Fig. 2b, #10); and providing an inspection item database section (col. 6, ll. 4-7, database 3) in which a circuit feature of said semiconductor integrated circuit corresponds to at least one inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed (Fig. 1, #104), wherein said circuit design unit generated circuit feature information indicating said circuit feature of said semiconductor integrated circuit for which said logical design should be executed (col.

6, ll. 56-65; see also col. 13, ll. 23-48) wherein said circuit design unit obtains a certain inspection item of said at least one inspection item, said certain inspection item corresponding to said circuit feature information from said inspection item database section (col. 7, ll. 10-17; col. 13, ll. 23-48), wherein said circuit design unit executes said logical design of said target semiconductor integrated circuit with reference to said certain inspection item (col. 7, line 66 to col. 8, line 19).

11. Pursuant to claims 17, further comprising providing a layout design unit executing said layout design (Fig. 2b, manufacture section), wherein said circuit design unit executes said inspection of said semiconductor integrated circuit for which said layout design is executed (col. 13, ll. 23-47), with regard to said certain inspection item, and wherein said circuit design unit provides a result of said inspection of said semiconductor integrated circuit to said layout design unit (col. 7, ll. 56-65).

12. Pursuant to claim 20, wherein said inspection item database section is connected to said circuit design unit (Figs. 2a, 2b).

Allowable Subject Matter

13. Claims 2, 4, 5, 7, 9, 10, 16, 18 and 19 are allowed.

14. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach a model development history database in which an

ID data of the circuit design unit corresponds to the number of inspection failures of the inspection item by the circuit design unit. .

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a complete listing.

17. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

18. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

A. M. Thompson
Primary Examiner
Technology Center 2800